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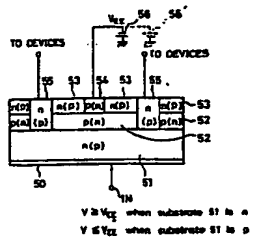
(54) Semiconductor integrated circuit having interconnection with improved design flexibility.

(57) A semiconductor integrated circuit comprises a substrate (51) of a first semiconductor type doped by a first impurity element with a first impurity density, the first semiconductor type being one of p-type and n-type semiconductors, a conductive layer (50) formed on a back surface of the substrate, a first layer (52) of a second semiconductor type doped by a second impurity element different from the first impurity element and formed on a front surface of the substrate, the second semiconductor type being the other of the p-type and n-type semiconductors and the first layer having a second impurity density lower than the first impurity density, a second layer (53) of the first semiconductor type formed on the first layer for forming circuit elements therein, a first region (54) of the second semiconductor type extending from a top surface of the first layer and reaching a top surface of the second layer, and a second region (55) of the first semiconductor type extending from a top surface of the substrate and reaching the top surface of said second layer, the first layer and the second region forming a conductive path for supplying a power source voltage to the circuit elements in the second layer from the back surface of the substrate.

FIG. 4



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SEMICONDUCTOR INTEGRATED CIRCUIT HAVING INTERCONNECTION WITH IMPROVED DESIGN FLEXIBILITY

BACKGROUND OF THE INVENTION

The present invention generally relates to semiconductor integrated circuits, and more particularly to a bipolar semiconductor integrated circuit.

The integration density of semiconductor integrated circuits is rapidly increasing due to the progress of various lithography and related techniques. Hence, the number of signal interconnections within the integrated circuit is increasing, and a region for providing power source interconnections for supplying power source voltages is increasing because of the increase in the power consumption of the integrated circuit. Especially in the case of a bipolar integrated circuit, it is impossible to reduce the current consumption of each circuit below a predetermined value in order to maintain the high-speed operation of each circuit.

In addition, the number of multi-level interconnections is limited to approximately three because problems such as disconnection or inconsistent thickness of the interconnection are easily caused when four or more levels of interconnections are stacked. Consequently, the chip size becomes large because of the need to increase the signal interconnections in each level and to widen the power source interconnections. Hence, there is a demand to prevent such an increase of the chip size. On the other hand, when the length of the signal interconnection is long, it is impossible to realize a high-speed circuit operation even when high-speed circuit elements are used.

FIGS.1A and 1B are a plan view and a cross sectional view respectively showing an example of a conventional semiconductor integrated circuit. In FIGS.1A and 1B, a semiconductor chip 12 is accommodated within a stage 11 of a package 10. Terminals 13 for signal input and output and terminals 14 for supplying power source voltages V_{CC} and V_{EE} are provided on the semiconductor chip 12, and these terminals 13 and 14 are wire-bonded on package leads 15.

A first power source interconnection (not shown) for the power source voltage V_{CC} and a second power source interconnection 16 for the power source voltage V_{EE} are provided on the semiconductor chip 12. The first and second power source interconnections respectively have stripe patterns which intersect each other in the plan view. For example, an emitter coupled logic (ECL) circuit is formed between the first and second power source interconnections.

FIG.2 shows a cross sectional view of the semiconductor chip 12. As shown in FIG.2, the semiconductor chip 12 has a p^--type substrate 21 provided with a metallized layer 20 on a back surface thereof. An n^+-type buried layer 22, an n-type epitaxial layer 23, a p^+-type isolation layer 24, a p-type diffusion layer 25 which becomes a base, an n^+-type diffusion layer 26 which becomes an emitter, an n^+-type diffusion layer 27 which becomes a collector, and a p-type diffusion layer 28 which becomes a resistor, are provided on a front surface of the p^--type substrate 21. In addition, the semiconductor chip 12 has insulator layers 29 and 30 indicated by hatchings, a first interconnection 31, and a second interconnection 32. For example, the second interconnection 32 corresponds to the second power source interconnection 16 for the power source voltage V_{EE} shown in FIGS.1A and 1B.

When considering an integrated circuit with 1000 gates where the current consumption is 1 mA per gate, for example, a current of 1 A flows in total. When the power source interconnection is an aluminum interconnection having a current density of 2×10^5 A/cm^2 and a thickness of 1 micron, the power source interconnection needs a large width of 0.5 mm. In addition, there are problems in that a voltage drop caused by the large current flow is large in the power source interconnection having the stripe pattern and that the noise margin of the circuit is poor.

Because of the need to reduce the capacitance between the collector and the substrate, that is, mainly the capacitance introduced between the n^+-type buried layer 22 and the substrate 21, the substrate 21 has a low impurity density with a high resistivity in the range of 5 Ωcm to 30 Ωcm. Normally, the substrate 21 has a thickness of 500 microns, and for this reason, it is impossible to supply the power source voltage from the back surface of the substrate 21 when the voltage drop is taken into account. Thus, the first and second interconnections 31 and 32 are used to supply the power source voltages.

Therefore, the conventional semiconductor integrated circuit suffers problems in that the voltage drop is large due to the long power source interconnections, and the freedom with which the signal interconnections may be designed is limited because the signal interconnections must be positioned avoiding the power source interconnections. In other words, the design flexibility of the interconnection is poor in the conventional integrated circuit. Furthermore, there is another problem in that the chip size becomes large because of the need

to provide a large number of terminals for the power source voltages on the semiconductor chip.

In order to overcome the problem, the applicant has proposed a semiconductor integrated circuit in the Japanese Laid-open Patent Application No.01-73669 published on March 17, 1989 and corresponding to the United States Patent Application S.N.243,745 filed September 13, 1988, European Patent Application No.88114886.0 filed September 12, 1988 and Korean Patent Application No.88-11860 filed September 14, 1988, of which construction is shown in FIG.3.

Referring to FIG.3, the proposed device has a p^+-type substrate 41 having a high impurity density with a resistivity of 0.1 Ωcm or less. A metallized layer (conductive layer) 42 is provided on a back surface of the p^+-type substrate 41. A p^--type epitaxial layer (first p-type layer) 43 having a high resistivity in the range of 1 Ωcm to 30 Ωcm is formed on a front surface of the p^+-type substrate 41. A p^+-type layer (second p-type layer) or region 44 having a low resistivity is selectively formed within the p^--type epitaxial layer 43.

Similarly as in the case of the conventional semiconductor chip shown in FIG.2 described before, an n^+-type buried layer 22a, an n-type epitaxial layer 23a, a p^+-type isolation layer or region 24a, a p-type diffusion layer 25a which becomes a base, an n^+-type diffusion layer 26a which becomes an emitter, an n^+-type diffusion layer 27a which becomes a collector contact, and a p-type diffusion layer 28a which becomes a resistor are provided on the front surface of the p^+-type substrate 41. In addition, the semiconductor chip has insulator layers 29a and 30a indicated by hatchings, a first interconnection 31a, and a second interconnection 32a.

Hence, a conductor path is formed from the metallized layer 42 to the first and second interconnections 31a and 32a through the p^+-type substrate 41 having the low resistivity, the p^+-type layer 44 and the p^+-type isolation layer 24a. The second interconnection 32a is connected to transistors and resistor elements formed on the substrate surface.

According to the semiconductor integrated circuit of this previous proposal, the length of the power source interconnection is shortened and the voltage drop can be decreased compared to the conventional semiconductor integrated circuit. In addition, the noise margin is improved and it is possible to realize a high-speed circuit operation. Moreover, because the conductor path for supplying the power source voltage is arranged vertically on the substrate, the signal interconnections can be designed with a large degree of freedom, thereby making it possible to prevent the chip size from increasing.

In this previous semiconductor integrated circuit, however, there arises a problem in that the voltage applicable to the substrate 41 via the metallized layer 42 is limited to a low voltage. Note that there is formed a p-n junction in this structure as shadowed in FIG.3 between the region 24a and the layer 23a, and the current is leaked into the layer 23 and further to the layer 27a through the p-n junction when the voltage applied to the metallized layer 42 has exceeded the threshold voltage of the p-n junction. Such a forward biasing of the p-n junction can occur when the voltage at the epitaxial layer 23a becomes lower than the voltage at the p^+-type isolation layer 24a in response, for example, to the collector voltage appearing in the region 27a. Thus, in order to avoid the undesirable forward biasing of the p-n junction, it is necessary to maintain the voltage at the layer 24a and hence the voltage applied to the metallized layer 42 as low as possible. As a matter of fact, the voltage applicable to the metallized layer 42 is limited to the most negative voltage used in the integrated circuit.

A similar problem occurs also in the case that the conductive type of the semiconductor layers in FIG.3 is reversed. In this case, the voltage applicable to the metallized layer 42 is limited to the most positive voltage used in the integrated circuit. Hence, the integrated circuit of FIG.3 has a problem in that the degree of freedom of circuit design is substantially limited.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide a novel and useful semiconductor integrated circuit in which the foregoing problems are eliminated.

Another and more specific object of the present invention is to provide a semiconductor integrated circuit comprising a substrate of a first conductive type, a first semiconductor layer of a second conductive type provided on the substrate, and a second semiconductor layer of the first conductive type provided on the first semiconductor layer and on which active device or devices are provided, wherein there is provided an isolation region having the second conductive type in the second semiconductor layer and wherein a conductive region of the first conductive type is provided such that the conductive region extends from the substrate throughout the second and first semiconductor layers until to the top surface of the second semiconductor layer. The isolation region is applied either with the highest positive voltage or lowest negative voltage such that the p-n junction formed between the isolation region and the sec-

ond semiconductor layer surrounding the isolation region is maintained in the reversely biased state while the conductive region is used for supplying the electric current to the active device or devices at the surface of the second semiconductor layer. According to the semiconductor integrated circuit of the present invention, it is possible to apply various voltages to the active device or devices on the second semiconductor layer in contrast to the prior art device. Further, the length of a power source interconnection is reduced and a voltage drop is effectively reduced thereby. In addition, it is possible to reduce the power source interconnections on the surface of a semiconductor chip. As a result, signal interconnections may be designed with a large degree of freedom and it is possible to prevent the chip size from increasing. The biasing of the isolation region does not complicate the construction of the device as such a biasing does not require substantial current and the connection to the isolation region can be made by a thin conductor stripe.

Other objects and further features of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS.1A and 1B are a plan view and a cross-sectional view respectively showing an example of a conventional semiconductor integrated circuit;

FIG.2 is a cross sectional view of a semiconductor chip shown in FIGS.1A and 1B;

FIG.3 is a cross sectional view showing another semiconductor chip proposed previously by the applicant;

FIG.4 is a schematical view showing the fundamental structure of the integrated circuit of the present invention;

FIG.5 is a cross-sectional view showing the structure of semiconductor integrated circuit according to a first embodiment of the present invention;

FIGS.6A and 6B are a plan view and a cross-sectional view respectively showing the first embodiment of the semiconductor integrated circuit according to the present invention;

FIG.7 is a circuit diagram showing an ECL circuit within the semiconductor chip shown in FIGS.6A and 6B;

FIG.8 is a plan view with an enlarged scale showing interconnections for realizing the ECL circuit shown in FIG.7;

FIGS.9A - 9H are cross-sectional views showing fabrication process of the integrated circuit of FIG.5;

FIG.10 is a cross-sectional view showing a second embodiment of the integrated circuit of the present invention; and

FIGS.11A - 11E are cross-sectional views showing fabrication process of the integrated circuit of FIG.10.

DETAILED DESCRIPTION

First, the principle of the present invention will be described with reference to FIG.4 showing a schematical view of the essential part of the integrated circuit of the present invention. For the sake of clarity of the explanation and drawing, only the essential part is illustrated.

Referring to FIG.4, the integrated circuit of the present invention comprises a substrate 51 of the n-type or the p-type, and on which bottom surface, a metallization layer 50 is provided. In the following description, it is assumed that the substrate 51 is doped to the n-type. In the case that the substrate 51 is doped to the p-type, the conductive type of the semiconductor layers appearing in the drawing should be reversed.

On the substrate 51, a first semiconductor layer 52 of the p-type and having a high resistivity is provided and on the first semiconductor layer 52, a second semiconductor layer 53 of the n-type is provided. Further, an isolation layer 54 of the p-type is formed in the second semiconductor layer 53 so as to be surrounded by the n-type semiconductor material forming the second semiconductor layer 53. Further, a conductive region 55 of the n-type is formed through the first and second semiconductor layers 52 and 53 so as to extend from the substrate 51 to the surface of the second semiconductor layer 53.

In operation, the metallized layer 51 is connected to an input terminal IN to which a suitable voltage is applied, while the isolation region 54 is connected to a bias voltage source 56 which applies the most negative voltage or the source voltage V_{EE} used in the integrated circuit to the isolation region 54. In response thereto, the p-n junction formed between the isolation region 54 and the rest of the second semiconductor layer 53 is biased strongly in the reverse direction and this reversely biased state is maintained during the operation of the integrated circuit. Even when the voltage applied to the input terminal IN is higher than V_{EE}, the reversely biased state is maintained or even enhanced. Thus, a desired source voltage applied to the input terminal IN is supplied to the desired device or devices via a path passing through the conductive region 55 without leaking to other region in the second semiconductor layer 53. Further, because of existence of capacitance along the

boundary between the substrate 51 and the first semiconductor layer 52, any fluctuation of the source voltage is compensated and the operation of the devices in the integrated circuit is stabilized.

In the case that the substrate 51 is doped to the p-type, the region 54 is applied with a highest voltage used in the integrated circuit by another bias voltage source 56' providing the bias voltage with an opposite polarity and the reverse biasing to the p-n junction is maintained.

Next, a first embodiment of the semiconductor integrated circuit of the present invention will be described with reference to FIG.5.

Referring to FIG.5, the device has an n^+-type substrate 61 of a semiconductor chip 60 having a high impurity density with a resistivity of 0.1Ωcm or less. A metallized layer (conductive layer) 62 is provided on a back surface of the n^+-type substrate 61. A p^--type epitaxial layer (first p-type layer) 63 having a high resistivity in the range of 1Ωcm to 30Ωcm is formed on a front surface of the n^+-type substrate 61. An n^--type epitaxial layer (second n-type layer) 64 having a high resistivity is provided further on the first p-type layer 63, and a p^+-type conductive region 65 is selectively formed within the n^--type epitaxial layer 64 in continuation to the first p-type layer 63. Alternatively, the layer 63 may be formed by ion implantation.

Similarly to the case of conventional semiconductor chip shown in FIG.3 described before, an n^+-type buried layer 66 is formed under the n^--type epitaxial layer 64 including a part of the layer 64, an n^+-type conductive layer or region 67 formed selectively in a part of the remaining part 64a of the n^--type epitaxial layer 64 in correspondence to a location above the buried layer 66 so as to continue to the buried layer 66, the remaining part 64a of the n^--type epitaxial layer 64 acting as the collector of a pnp-transistor Tr formed on the chip 60, a p-type diffusion layer 68 formed in the surface part of the n^--type epitaxial layer 64 as the base, and an n^+-type diffusion layer 69 further defined in the p-type diffusion layer 68 as the emitter.

The surface of the chip 60 is provided with a field oxide layer 70 for device isolation except for the area of the chip on which the npn-transistor Tr is formed or the area where the p^+-type isolation region 65 and the n^+-type conductive region 67 are exposed. In the illustrated example, the transistor Tr is isolated by isolation trench structures IS1 and IS2 which are of ordinary structure including the insulation and polysilicon region surrounded by the insulation. Description for the structures IS1 and IS2 will be omitted. Further, there is provided a U-groove 71 on the surface of the chip 60 such that the U-groove 71 extends from the surface of the chip to the substrate 61 through the layers 64 and 65. The side wall of the U-groove 71 is covered by an oxide layer which extends in continuation to the field oxide layer 70, and the groove 71 is filled with an n^+-type polysilicon to form a conductive region 73 which extends from the substrate 61 to the surface of the chip 60.

On the surface of the chip 60, there are provided electrodes 74, 75, 76 and 77 respectively in correspondence to the conductive region 73, p^+-isolation region 65, p-type diffusion layer 68 corresponding to the base, n^+-type diffusion layer 69 corresponding to the emitter, and the conductive region 67 connected to the collector contact of the transistor Tr. These electrodes are separated from each other by an insulator film 78 deposited on the surface of the chip 60.

Hence, a conductor path is formed from the metallized layer 62 to the surface of the chip through the n^+-type substrate 61 having the low resistivity and the n^+-type conductive region 73 and when a source voltage is supplied to the matallized layer 62, this source voltage is passed to the surface of the chip 60 via the conductive region 73. On the surface of the chip 60, various interconnection patterns 79 are provided and distributes the source voltage to the desired terminal of the device as will be described later.

When using the device of FIG.5, the device is placed on a stage 100 to which a source voltage and the like is applied and the electrode 74 covering the exposed region of the p^+-type conductive region 65 is applied with a most negative voltage V_{EE} used in the device. As a result, the p-n junction formed between the region 65 and the n^--type layer 64 surrounding the region 65, or the p-n junction formed between the p^--type layer 63 to which the region 65 is connected and the n^+-type substrate 61, is always biased reversely and prohibits the current supplied to the metallized layer 62 from an external voltage source from entering into the region above the p^--type layer 63. The p-n junction aforementioned is maintained in the reversely biased state as long as the voltage to the metallized layer 62 is higher than the voltage V_{EE} applied to the p^+-type conductive region and thus, any desired voltage satisfying this condition such as the source voltage V_{CC}, which may be the ground level voltage, can be supplied to the interconnection patterns 79 at the surface of the chip 60 via the stage 100, metallized layer 62, and the conductive region 73 without problem of the current leaking into the layer 63 and hence to various parts of the integrated circuit 60.

Associated with the structure of FIG.5, there is another advantage in that a capacitance is formed along the p-n junction between the layer 63 and the layer 61 and this capacitance acts as a shunt capacitance. Thereby, the capacitance absorbs any

fluctuation of the source voltage V_{CC} or V_{EE}. Thus, the operation of the device constructed on the power supply structure of FIG.5 is immune to the fluctuation of source voltage and operates with improved stability.

The oxide layer at the side wall of the U-groove 71 is provided for increased insulation between the region 73 and the surrounding region and may be omitted.

The semiconductor chip 60 having the structure shown in FIG.5 is mounted on the stage 100 of a package 101 as shown in FIGS.6A and 6B. FIGS.6A and 6B are plan view and cross-sectional view respectively showing the first embodiment of the semiconductor integrated circuit according to the present invention in a state that the integrated circuit is mounted on the package 101.

In FIGS.6A and 6B, the semiconductor chip 60 is placed on the stage 100 provided in the package 101. The stage 100 may be a metallization provided on the package 101 and is connected to package leads 104 for the power source voltage V_{CC}. The semiconductor chip 60 is connected electrically to the package 101 via the metallized layer 62 in contact with the metallized layer 100 of the package 101. Further, terminals 105 for signal input and output and terminals 106 for supplying the power source voltage V_{EE} are provided on the semiconductor chip 70, and these terminals 105 and 106 are connected to package leads 107 by wire-bonding or the like. Note that the terminal 106 is connected to the electrode 74 covering the p^+-type region 74 by conductor patterns (not shown) on the surface of the chip 60.

One advantage of the present construction is that the distribution of the source voltage V_{EE} to various electrodes 73 on the chip does not require passage of the substantial current. Thus, such wiring to the electrode 73 can be achieved by thin conductor stripe without causing complexity in wiring of the chip.

Accordingly, the power source voltage V_{CC} is supplied to the semiconductor chip 60 through the package lead 104, the metallized layer 100 and the metallized layer 62 while under the reverse bias to the p-n junction between the n^+-type substrate 61 and the p^--type layer 63 due to the power source voltage V_{EE} applied to the terminal 106 and hence to the electrode 74 covering the p^+-type region 74, and thereby the power source voltage V_{CC} is passed through the n^+-type substrate 61 and the n^+-type region 73 to the interconnection conductor 79. Finally, the power source voltage V_{CC} thus directed to the surface of the chip 60 is distributed to the active device such as the ECL circuit or the like within the semiconductor chip 60 through the interconnection conductor 79. In FIG.6A, interconnections for supplying the power source voltage V_{CC} to the interconnection conductor 79 at the semiconductor chip 60 are shown by a numeral 108. This interconnection 108 corresponds to the electrode covering the exposed surface of the conductive region 73 of FIG.5 to which the interconnection conductor 79 is connected.

The interconnections 108 each occupy a small area and are scattered in the plan view in FIG.6A in a row and column formation in correspondence to the active devices formed on the substrate 61 of the chip. Hence, the signal interconnections may be provided between the interconnections 108 as indicated by arrows 109, and the signal interconnections may be designed with a large degree of freedom. The power source voltage V_{CC} is supplied from the back surface of the semiconductor chip 60 in correspondence to the position of the circuit which requires the power source voltage V_{CC}. In other words, the power source voltage V_{CC} is supplied to the circuit in a vertical path in the cross sectional view. For this reason, it is possible to make the interconnection for supplying the power source voltage V_{CC} extremely short. In addition, because the probability of a signal interconnection intersecting a power source interconnection is considerably reduced, it is possible to shorten the signal interconnection owing to the fact that there is less need to make a roundabout route to avoid intersecting the power source interconnection. As a result, it is possible to realize a high-speed circuit operation.

By biasing the p-n junction between the n^+-type substrate 61 and the p^--type layer 63 by the source voltage V_{EE} which is the most negative voltage used in the integrated circuit, the p-n junction is always biased in the reversed direction the penetration of current to various active devices constructed on the chip directly from the substrate 61 is positively prevented. In biasing the p-n junction, it should be noted that no substantial current is needed to flow through conductor pattern connecting the terminal 106 to the electrode 74 on the surface of the chip 60, and thereby such conductor pattern can be provided by using an extremely thin conductor stripes. In other words, the provision of the conductor pattern for biasing the p-n junction does not introduce complexity of wiring on the surface of the chip.

As a result of the construction as such, the voltage supplied to the surface of the chip 60 via the metallized layer 62 and the conductive region 73 is no longer limited to V_{EE} as in the case of the prior art of FIG.3 but the source voltage V_{CC} or any other voltage higher than the source voltage V_{EE} may be employed. Thereby, an increased freedom of design of the integrated circuit becomes possible.

The resistivity of the conductive path in the

semiconductor chip 60 from the metallized layer 62 to the interconnection conductor 79 through the n^+-type substrate 61 and the n^+-type conductive region 73 can be appropriately selected by changing the cross sectional area and/or the density of the n-type impurity of the conductive path and/or the thickness of the n-type layer 73.

For example, when the cross sectional area s of the conductive path is 100 m^2, the length L of the conductive path 5 microns and the resistivity ρ of the conductor path 0.01 Ωcm, a resistance R of the conductive path becomes $R = \rho(L/s) = 5\Omega$. In this case, the voltage drop due to a current of 1 mA is 5 mV. In addition, when the n^+-type substrate 61 has a size of 5 mm by 5 mm and a thickness t of 0.5 mm and a resistivity of 0.01 Ωcm, a voltage drop V for the case where a current I of 1 A flows in total may be described by $V = RI = \rho(t/s)I$. Hence, this voltage drop V is approximately 2 mV. Therefore, a total voltage drop is approximately 7 mV which is considerably small compared to the conventional case where the total voltage drop would be 50 mV or more.

The connection of the semiconductor chip 60 to the package 101 is made by die-bonding the semiconductor chip 60 on the stage 100. Thus, the power source voltage V_{CC} can be stably supplied to the semiconductor chip 60 without wire-bonding.

The problem of electromigration will not occur because the length of the metal interconnection 79 for the power source voltage V_{CC} can be made short and the current density can be held small.

It is possible to realize a large scale integrated (LSI) circuit having a higher density because the number of power source interconnections extending horizontally are reduced. Furthermore, the reliability of the semiconductor integrated circuit is improved because of the reduced number of levels of interconnections.

Since the n^+-type substrate 61 has the high impurity density, it is possible to prevent the n-type substrate from being transformed into the p-type due to oxygen and carbon which are included in the silicon substrate when the substrate is sliced from an ingot grown by the Czochralski method.

FIG.7 is a circuit diagram showing an ECL circuit within the semiconductor chip 60. In FIG.7, transistors Tr1, Tr2, Tr3, Tr4 and resistors R1, R2 and R3 are connected as shown. V_{EE} denotes the most negative power source voltage, V_{BB} and V_{CS} denote reference voltages, GND denotes the ground voltage, IN denotes an input of the ECL circuit, and OUT denotes an output of the ECL circuit.

FIG.8 shows, in an enlarged scale, a plan view of the interconnections for realizing the ECL circuit shown in FIG.7 using the first embodiment of the semiconductor integrated circuit shown in FIG.5. In FIG.8, those parts which are the same as those corresponding parts in FIGS.5, 6A, 6B and 7 are designated by the same reference numerals, and description thereof will be omitted. In FIG.8, the interconnections are shown with hatchings. B, E and C respectively denote the base, emitter and collector of the transistors Tr1 through Tr4.

Next, the process of fabricating the integrated circuit of FIG.5 will be described with reference to FIGS.9A - 9E. In these drawings, these parts already described with reference to preceding drawings are given identical reference numerals and the description thereof will be omitted.

In a step of FIG.9A, a part of the p^--type layer 63 on the n^+-type substrate 61 is selectively subjected to ion implantation and a part of the buried layer 66 as well as a part of the n^+-conductive layer 67 are formed. In a step of FIG.9B, the n^--type layer 64 is grown on the layer 63 and thereby, the dopants in the already existing part of the layer 66 and the layer 67 are diffused into the layer 64. As a result, the buried layer 66 and the conductive region 67 are formed.

In a step of FIG.9C, a U-groove 71 is formed on the surface of the chip so as to extend through the layers 64 and 63 up to the substrate 61, and the structure is subjected to a thermal oxidation process. In response to the thermal oxidation, the oxide layer 72 is formed on the side wall of the U-groove 71 including the free surface. Further, the structure thus obtained is subjected to an etching process wherein a part of the oxide layer 72 at the bottom of the U-groove 71 as well as the part covering the free surface of the structure are removed. With this, a structure shown in FIG.9D is obtained.

Next, in a step of FIG.9E, the U-groove 71 is filled by a doped polysilicon 73 doped to the n^+-type which may be deposited by a CVD process. After removing superfluous polysilicon (not shown) on the surface of the structure of FIG.9E, the structure of FIG.9E is obtained.

Further, another U-grooves U1 and U2 are formed on the surface of the structure of FIG.9E to form a structure shown in FIG.9F, and the grooves U1 and U2 are filled by polysilicon as shown in FIG.9G. Next, the region 65 is formed by ion implantation followed by heat treatment and the structure shown in FIG.9H is obtained. On this structure, the field oxide layer 70 is provided as usual, and the npn-transistor Tr of FIG.5 is formed according to the well established process.

FIG.10 shows a second embodiment of the semiconductor integrated circuit according to the present invention. In FIG.10, these parts identical to those corresponding parts described previously with reference to preceding drawings are given identical reference numerals and the description

thereof will be omitted.

In the structure of FIG.10 showing a chip 60a, an n^+-type conductive region 73a is provided in place of the conductive region 73. This region 73a is formed by ion implantation and annealing repeated each time the layers 63 and 64 are grown as will be described. As the region 73a is formed by ion implantation, the conductive region 73a is not surrounded by the insulating side wall 72, and the voltage such as V_{CC} at the bottom of the chip 60a is passed to an electrode 79a at the top of the chip 60a.

In this embodiment, in place of the p^+-type conductive region 65, a U-groove 65a extending from the surface of the layer 64 to the layer 63 is formed. An oxide layer 71a is formed on the side wall of this groove 65a, and the groove is filled by a p^+-type polysilicon 65b. On the exposed top surface of the polysilicon region 65b, an electrode 74a corresponding to the electrode 74 of FIG.5 is provided and through this electrode 74, the source voltage V_{EE} is applied. In response to the source voltage V_{EE}, the p-n junction at the boundary between the substrate 61 and the p^--type epitaxial layer 63 is biased reversely and penetration of the current to the region under the transistor Tr5 is prevented.

In this construction, there is another npn transistor Tr6 of which collector is connected to an n^+-type region 73b provided in continuation to the n^+-type substrate 61. Thus, the source voltage V_{CC} is supplied directly to the collector of the transistor Tr6 through the conductive region 73b.

Next, the process of fabricating the integrated circuit of FIG.10 will be described with reference to FIGs.11A - 11E. In these drawings, those parts identical to the parts already described with reference to preceding drawings are given identical reference numerals and the description thereof will be omitted.

In a first step of FIG.11A, a layered structure comprising the substrate 61, the p^--type epitaxial layer 63, the n^--type epitaxial layer 64, the n^+-type conductive regions 73a and 73b, and the buried layer 66 is formed. Next, U-grooves 65a, U1 and U2 are formed such that each of the grooves extend from the surface of the structure to the layer 63. The grooves U1 and U2 are formed at both lateral ends of the buried layer 66 and all of the grooves have side walls covered by an oxide insulator layer.

In the step of FIG.11C, the insulator layer at the bottom of the groove 65a is removed, and in the step of FIG.11D, a polysilicon doped to the p^+-type is deposited such that the grooves 65a, U1 and U2 are filled by the polysilicon. Thereby, the conductive region 65b is formed.

Further, ion implantation is made to the epitaxial layer 64 in correspondence to the conductive region 73a and after annealing, another diffusion region 73c of the n^+-type is formed in continuation to the region 73a. Further, various devices such as the npn-transistors Tr5, Tr6 and the like are provided on the surface of the epitaxial layer 64 by well known process.

Further, the present invention is not limited to these embodiments described heretofore but various variations and modifications may be made without departing from the scope of the present invention.

Claims

1. A semiconductor integrated circuit comprising a substrate (51) of a first semiconductor type doped by a first impurity element with a first impurity density, said first semiconductor type being one of p-type and n-type semiconductors, a conductive layer (50) formed on a back surface of said substrate,
characterized by a first layer (52) of a second semiconductor type doped by a second impurity element different from the first impurity element and formed on a front surface of said substrate, said second semiconductor type being the other of the p-type and n-type and said first layer having a second impurity density lower than the first impurity density, a second layer (53) of the first semiconductor type formed on said first layer for forming circuit elements therein, a first region (54) of the second semiconductor type extending from a top surface of said first layer and reaching a top surface of said second layer, and a second region (55) of the first semiconductor type extending from a top surface of said substrate and reaching the top surface of said second layer, said first layer and said second region forming a conductive path for supplying a power source voltage to the circuit elements in said second layer from the back surface of said substrate.

2. A semiconductor integrated circuit as claimed in claim 1 characterized in that said first region (54) has an impurity density higher than that of the first layer (52).

3. A semiconductor integrated circuit as claimed in claim 1 characterized in that said second region (55) has an impurity density approximately equal to that of the substrate (51).

4. A semiconductor integrated circuit as claimed in claim 1 characterized in that said first region (65b) is surrounded laterally by an insulator layer (65a).

5. A semiconductor integrated circuit as claimed in claim 1 characterized in that said second region (73) is surrounded laterally by an in-

sulator (72).

6. A semiconductor integrated circuit as claimed in claim 1 characterized in that the semiconductor integrated circuit further comprises biasing means (56, 56′) connected to the first region (54) at the top surface of the second layer (53) for maintaining a p-n junction formed between the substrate (51) and the first layer (52) in a reverse biasing state, and said conductive layer (51) is adapted for connection to a voltage source.

7. A semiconductor integrated circuit as claimed in claim 6 characterized in that said first semiconductor type is the n-type, said second semiconductor type is the p-type, said biasing means applies (56) a first predetermined voltage (V_{EE}) set to the lowest voltage used in the semiconductor integrated circuit to the first region (54).

8. A semiconductor integrated circuit as claimed in claim 7 characterized in that said circuit element formed in the second layer comprises an npn transistor (Tr), and the semiconductor integrated circuit further has an interconnection structure (79) at the top surface of the second layer (64) for connecting the second region (73) to a collector of the npn transistor so as to supply a second predetermined voltage, supplied to the second region from a voltage source through the conductive layer and the substrate, to the collector as a source voltage (V_{CC}) .

9. A semiconductor integrated circuit as claimed in claim 8 characterized in that said first predetermined voltage supplied to the first region (54) by the biasing means (56′) is set to a second source voltage (V_{EE}) lower than the first source voltage (V_{CC}).

10. A semiconductor integrated circuit as claimed in claim 6 characterized in that said first semiconductor type is the p-type, said second semiconductor type is the n-type, said biasing means (56′) applies a first predetermined voltage set to the highest voltage (V_{EE}) used in the semiconductor integrated circuit to the first region at the surface of the second layer.

11. A method of fabricating a semiconductor integrated circuit comprising a layered semiconductor body including a path for supplying an electric current from a rear side of the layered semiconductor body to an active device on a front side of the layered semiconductor body through the layered semiconductor body, comprising steps of of providing a substrate (61) of a first semiconductor type, providing a first layer (63) of a second semiconductor type on the substrate so that there is formed a p-n junction between the substrate and the first layer, providing a second layer (64) of the first semiconductor type on the first layer,
characterized in that the method further comprises steps of providing a groove (71) such that the groove extends from a top surface of the second layer to the substrate through the first layer, filling the groove with a semiconductor material (73) having the first semiconductor type, so that a path of electric current is established from the substrate to the top surface of the second layer, and providing a region (65) of the second semiconductor type in a part of the second layer different from the part where the groove is formed such that the region reaches the first layer.

12. A method as claimed in claim 11 characterized in that the method further comprises a step of providing an insulator layer (72) on a side wall of the groove (71) prior to the step of filling the groove by the semiconductor material (73).

13. A method of fabricating a semiconductor integrated circuit comprising a layered semiconductor body including a path for supplying an electric current from a rear side of the layered semiconductor body to an active device on a front side of the layered semiconductor body through the layered semiconductor body, comprising steps of providing a substrate (61) of a first semiconductor type, providing a first layer (63) of a second semiconductor type on the substrate so that there is formed a p-n junction between the substrate and the first layer, forming a first region (73a) of the first semiconductor type in the first layer, providing a second layer (64) of the first semiconductor type on the first layer including the first region,
characterized by steps of providing a groove (65a) on the second layer such that the groove extends from a top surface of the second layer to the first layer, filling the groove by a semiconductor material (65c) of the second semiconductor type, and forming a second region (73c) of the first semiconductor type in the second layer in correspondence to the first region with an impurity density higher than that of the second layer such that the first region and the second region are connected.

14. A method as claimed in claim 13 characterized in that the method further comprises a step of providing an insulator layer (65b) on a side wall of the groove (65a) prior to the step of filling the groove.

FIG. 1A PRIOR ART

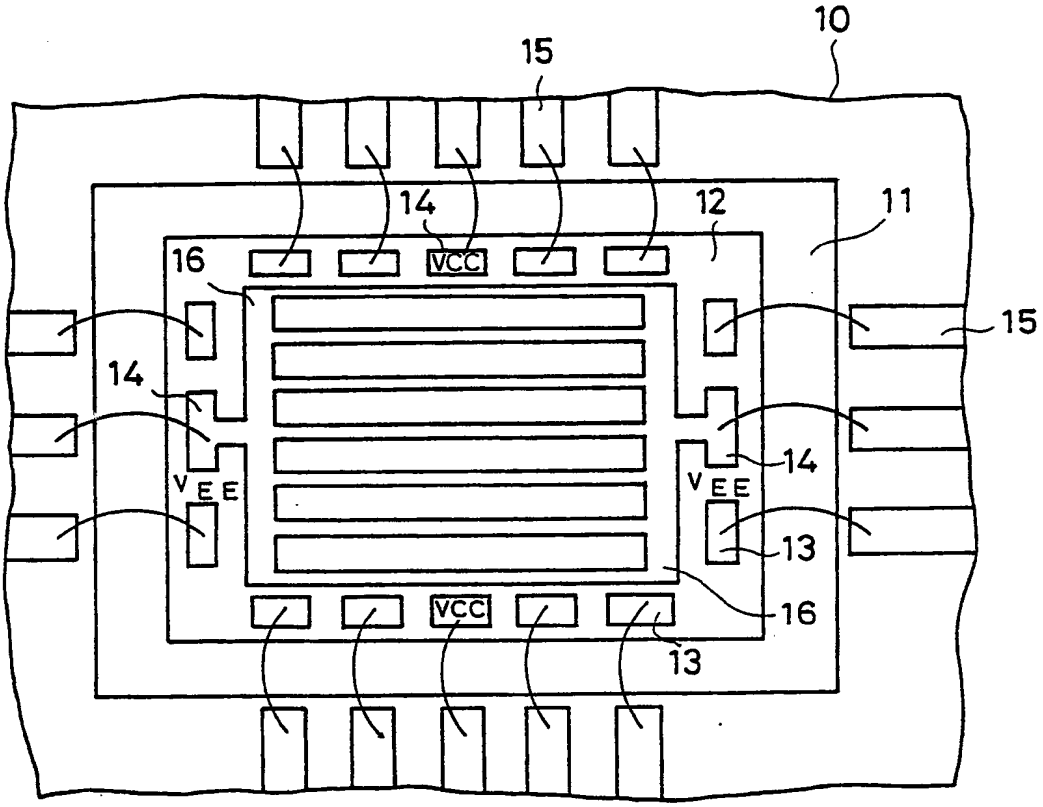
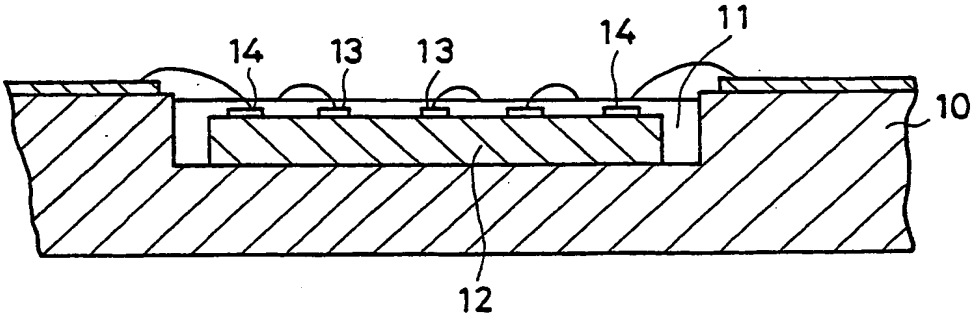


FIG. 1B PRIOR ART



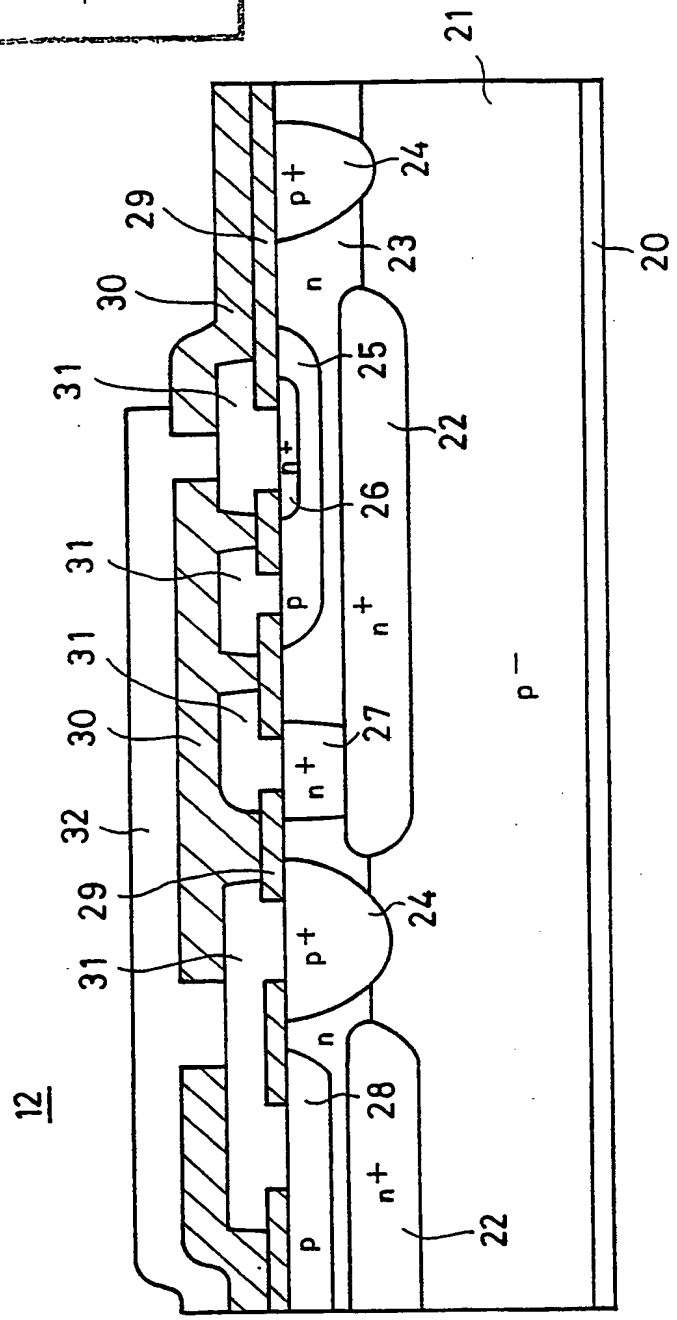


FIG.2 PRIOR ART

FIG. 3

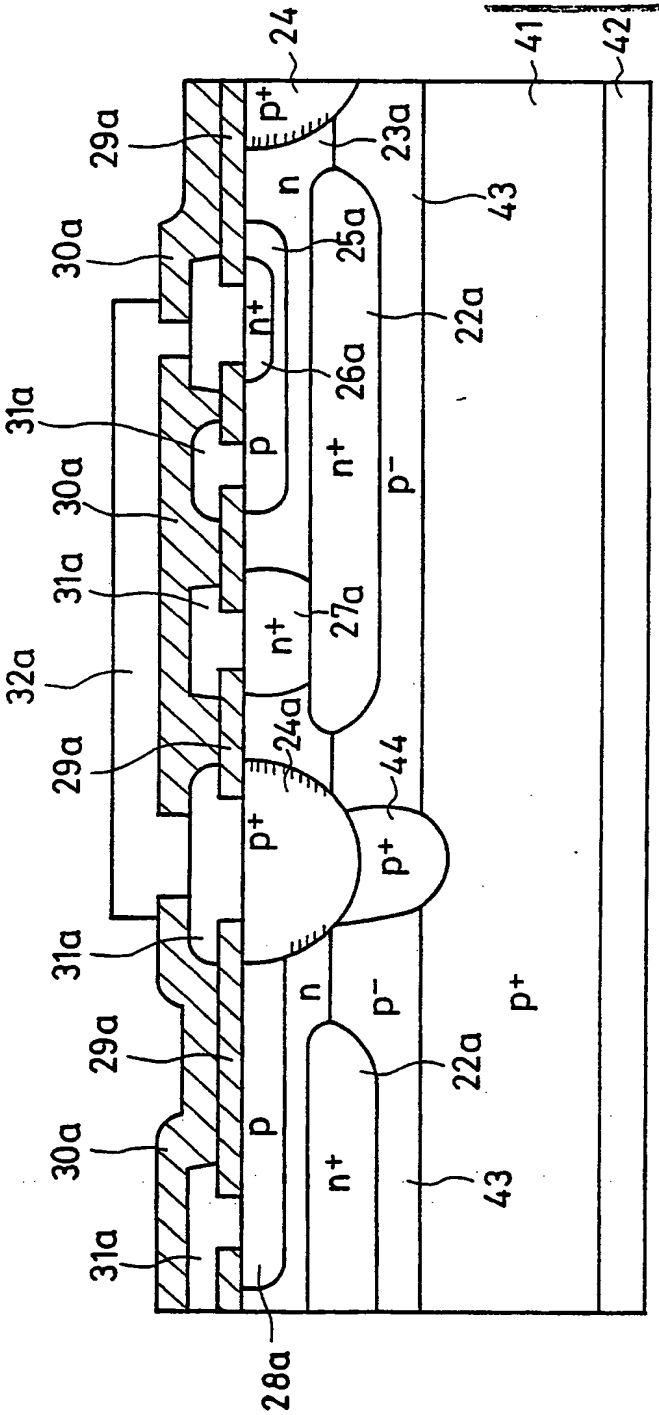
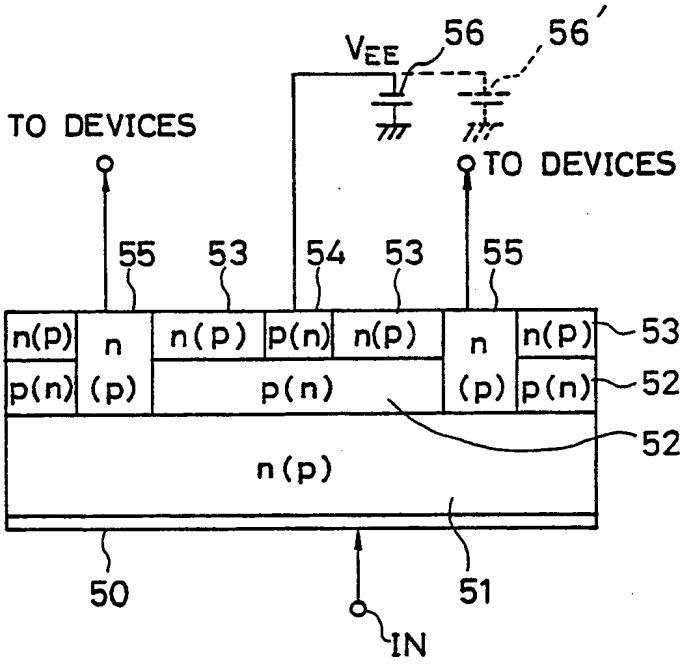


FIG. 4



$V \geq V_{EE}$ when substrate 51 is n

$V \leqq V_{EE}$ when substrate 51 is p

FIG. 5

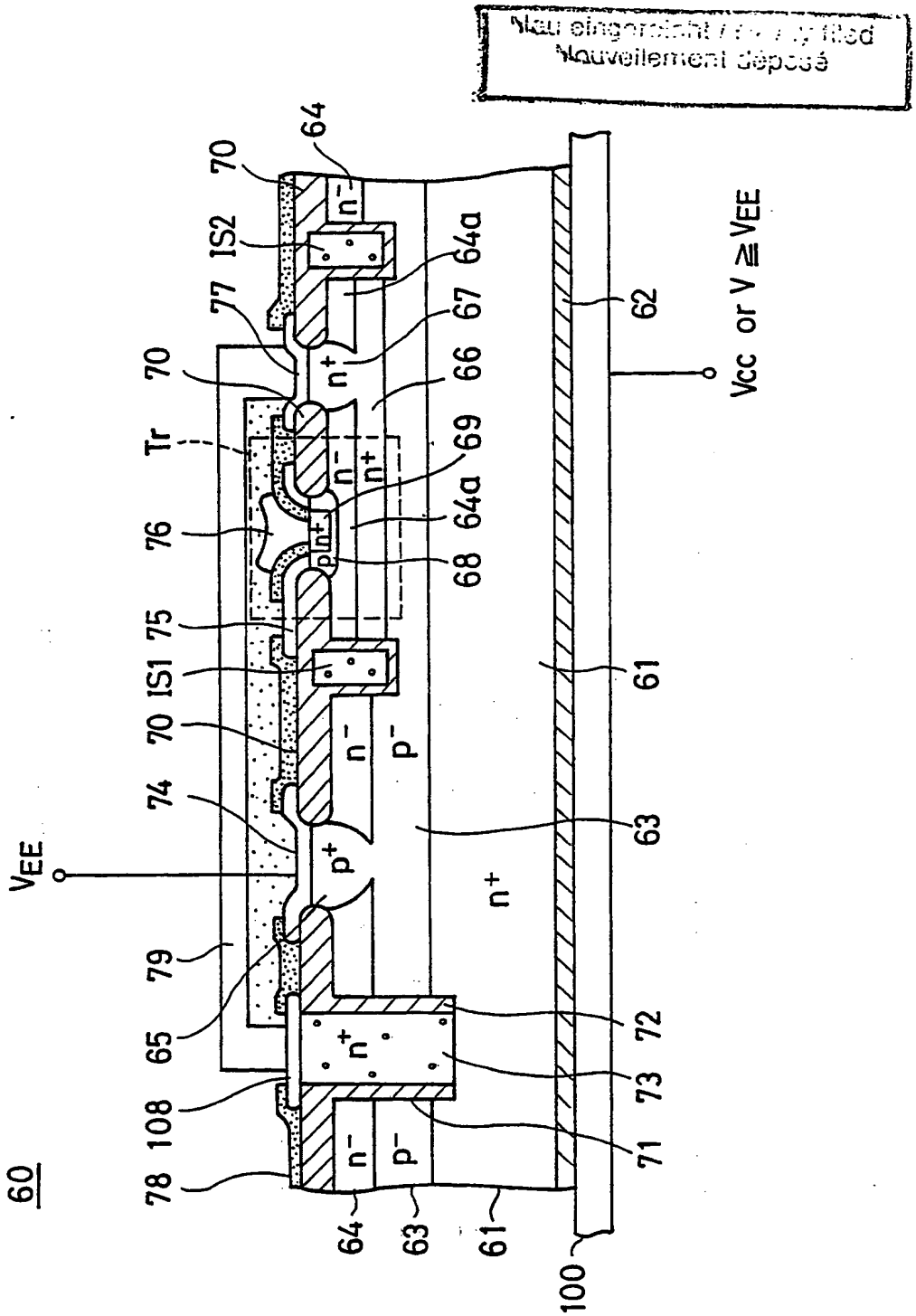


FIG. 6A

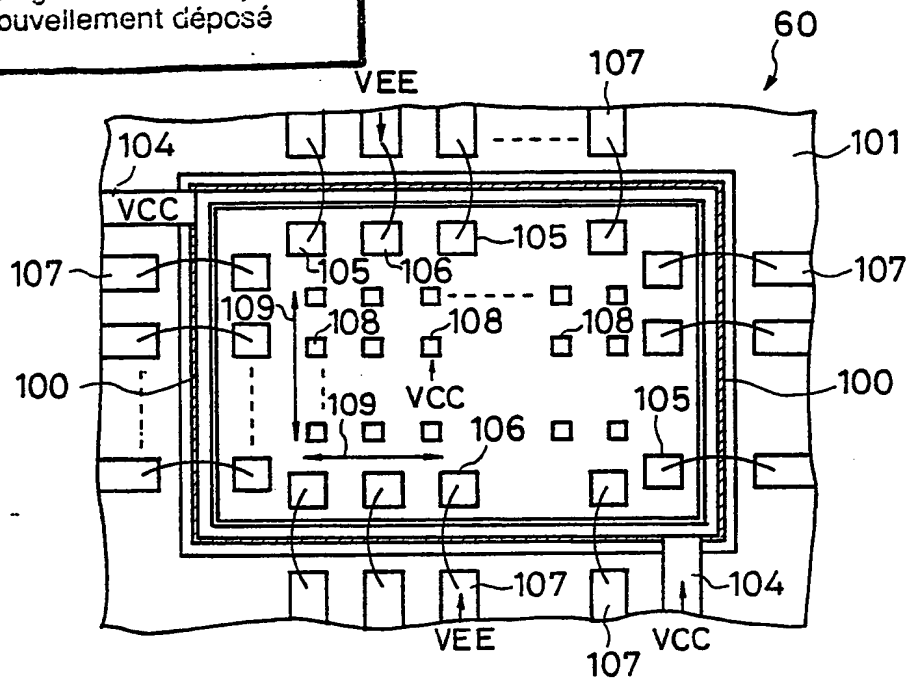


FIG. 6B

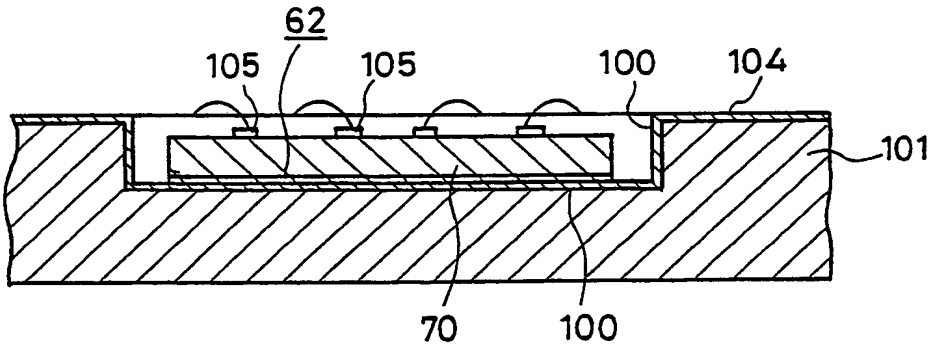


FIG. 7

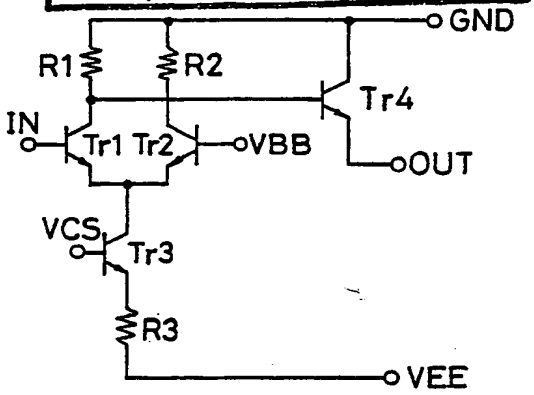
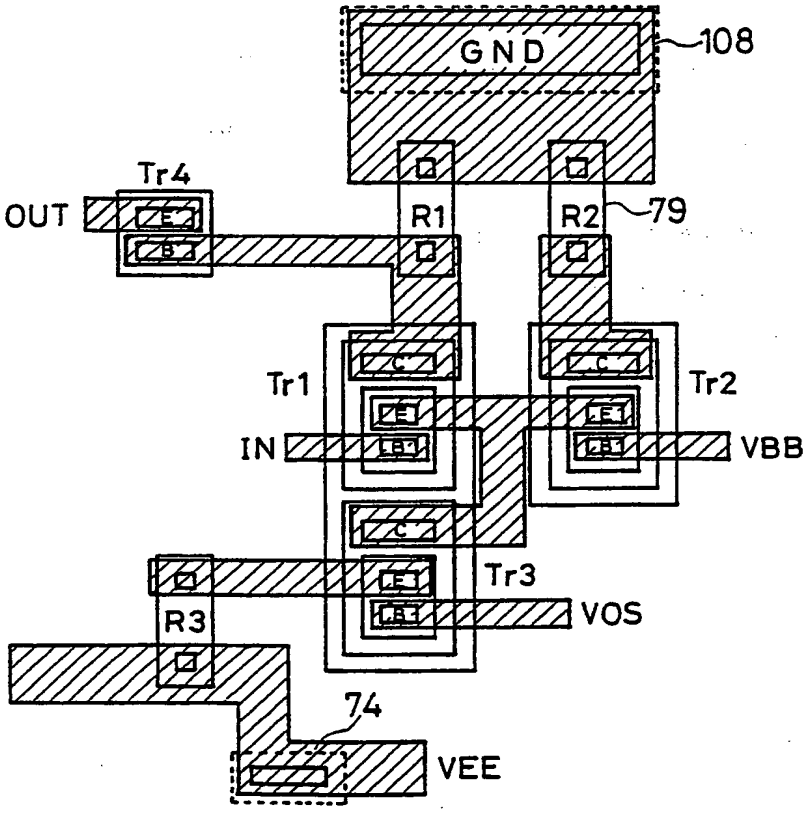


FIG. 8



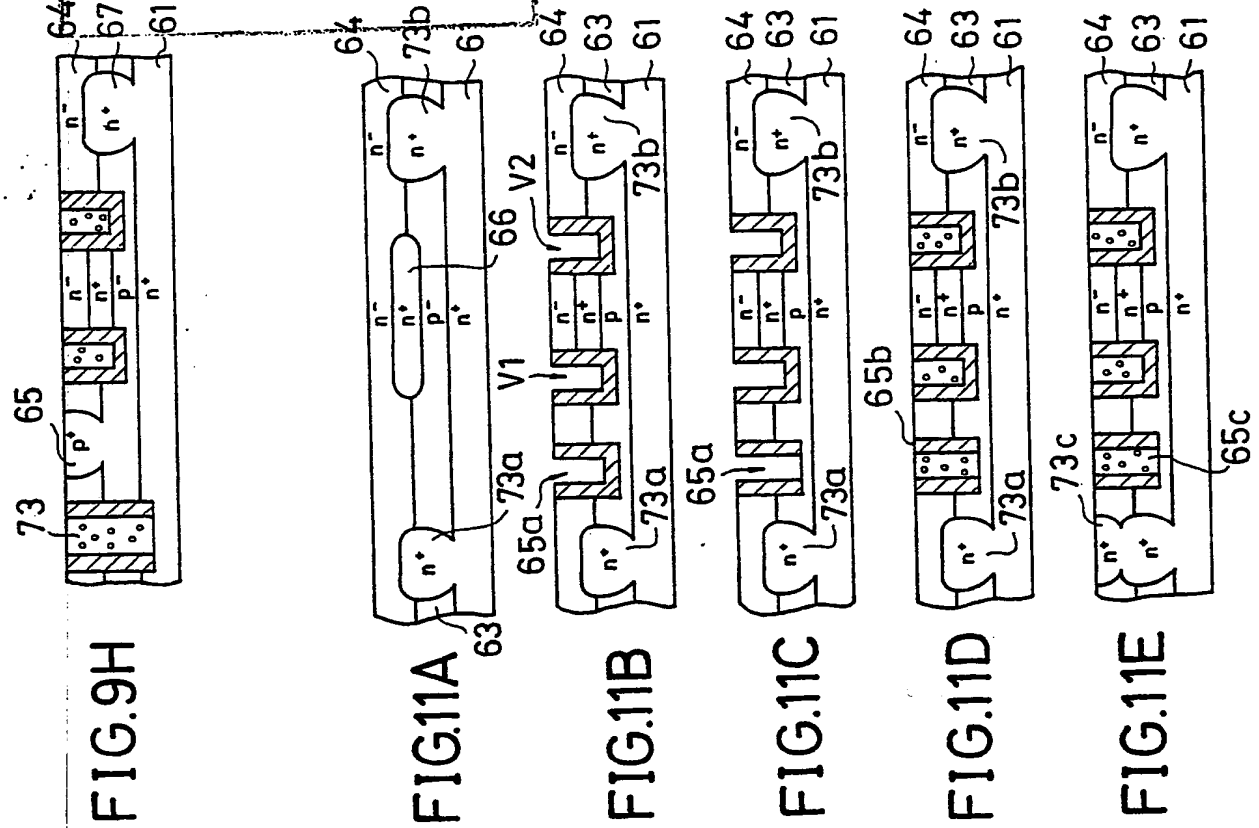


FIG.9H FIG.11A FIG.11B FIG.11C FIG.11D FIG.11E

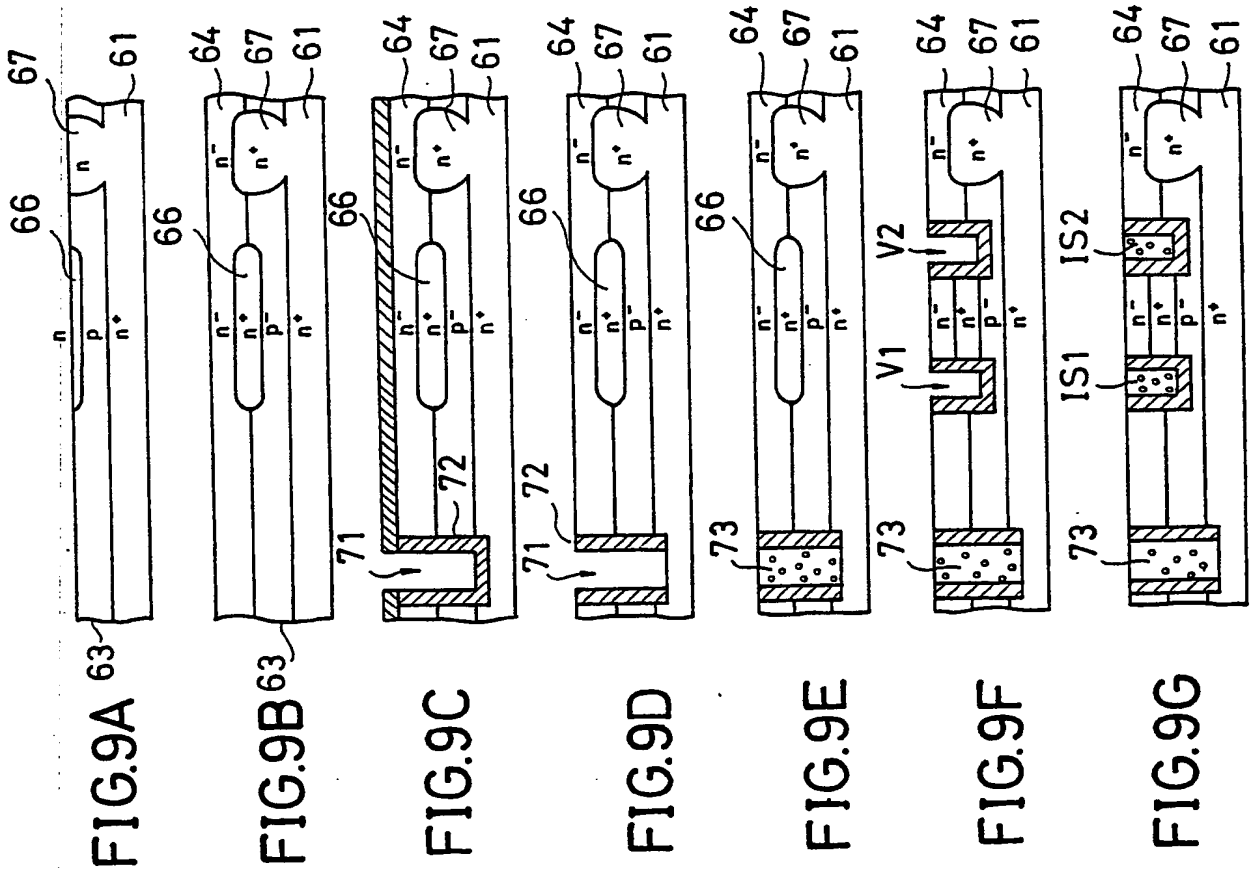


FIG.9A FIG.9B FIG.9C FIG.9D FIG.9E FIG.9F FIG.9G

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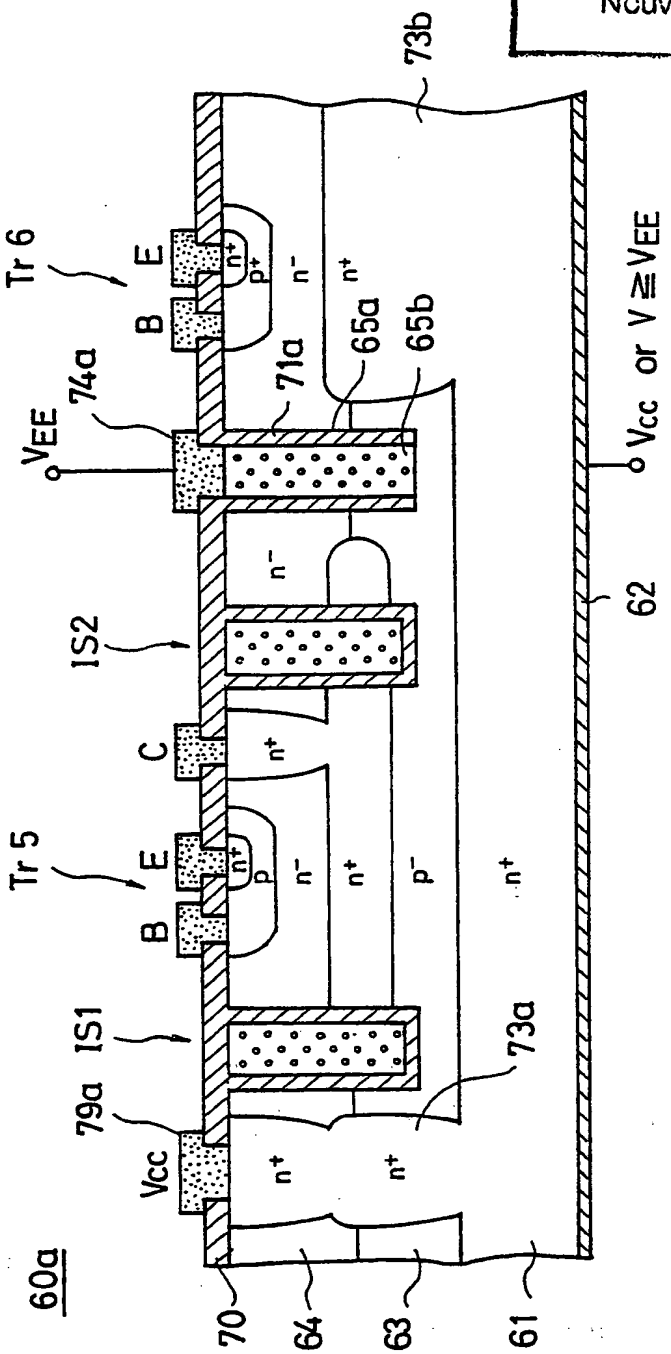
Nouvellement déposé

FIG. 10



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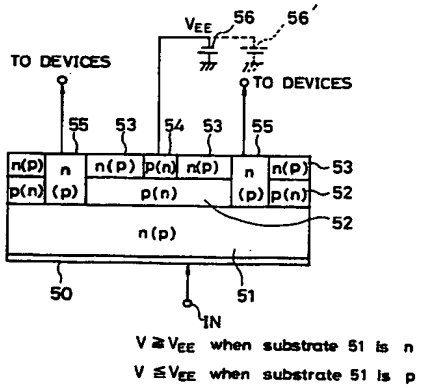
(54) Semiconductor integrated circuit having interconnection with improved design flexibility.

(57) A semiconductor integrated circuit comprises a substrate (51) of a first semiconductor type doped by a first impurity element with a first impurity density, the first semiconductor type being one of p-type and n-type semiconductors, a conductive layer (50) formed on a back surface of the substrate, a first layer (52) of a second semiconductor type doped by a second impurity element different from the first impurity element and formed on a front surface of the substrate, the second semiconductor type being the other of the p-type and n-type semiconductors and the first layer having a second impurity density lower than the first impurity density, a second layer (53) of the first semiconductor type formed on the first layer for forming circuit elements therein, a first region (54) of the second semiconductor type extending from a top surface of the first layer and reaching a top surface of the second layer, and a second region (55) of the first semiconductor type extending from a top surface of the substrate and reaching the top surface of said second layer, the first layer and the second region forming a conductive path for supplying a power source voltage to the circuit elements in the second layer from the back surface of the substrate.

FIG. 4



EP 0 382 504 A3

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EUROPEAN SEARCH REPORT

Application Number

EP 90 30 1286

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	FR-A-1 552 459 (MOTOROLA) * page 1, right column, last paragraph - page 4, left column, last paragraph; figures 1-7 *	1-3,6-9, 13	H01L23/522 H01L29/06 H01L27/06 H01L23/58
Y	* ditto *	11,12,14	
Y	EP-A-0 272 453 (TEXAS INSTRUMENTS INCORPORATED) * abstract; figures 1-6 *	11,12,14	
A	IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE, vol. 32, February 1989, NEW YORK US pages 182 - 183; NORIHITO MIYOSHI ET AL.: 'A 50k-Gate ECL Array with Substrate Power Supply' * the whole document *	1,11,13	
A	WO-A-8 600 755 (MOTOROLA) * page 3, line 29 - page 5, line 32; figure 2 *	1,11,13	
A	CH-A-493 097 (ITT INDUSTRIES) * column 5, line 14 - line 39; figures 6,7 *	1,11,13	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	18 JUNE 1992	LE MINH I.

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